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THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor : Eiki Hashimoto
Serial No : 10/015,209
Filed : November 16, 2001
Title : Semiconductor Circuit Designing Apparatus and...
Group Art Unit : 2812

June 27, 2002

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ORIGINALLY FILED

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Assistant Commissioner for Patents
Washington, D.C. 20231

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Any fee, due as a result of this paper may be charged on Deposit Account No. 50-1290.

Respectfully submitted,

Michael I. Markowitz
Reg. No. Reg. No. 30,659

Katten Muchin Zavis Rosenman
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575 Madison Avenue
New York, New York 10022-2585
Tel. (212) 940-8800
Docket No.: NEKU 19.181 (100806-00056)
sl

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DATE June 27, 2002



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UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, DC 20231
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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/015,209	11/23/2001	Eiki Hashimoto	NEKU 19.181

026304
KATTEN MUCHIN ZAVIS ROSENMAN
575 MADISON AVENUE
NEW YORK, NY 10022-2585

CONFIRMATION NO. 5984



OC000000008032538

Date Mailed: 05/06/2002

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Application Filing Date

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- ☐ The "date in" on the Express Mail label is the date given on the Filing Receipt.
- ☐ The filing date accorded to the application is the date the application met the filing date requirements of 37 CFR 1.53(b) or (c).
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Commissioner for Patents
Washington, DC 20231

Nepa Karopas

Customer Service Center
Initial Patent Examination Division
(703) 308-1202



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PATENTS
U.S. PTO

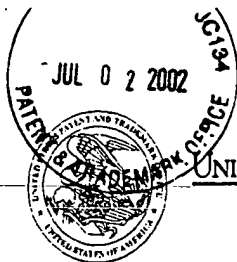
To: Assistant Commissioner for Patents
Serial/Patent No. **10/015209**
Filing date **11/16/01**
Inventor(s):
Title: A semiconductor circuit for timing apparatus and a method of determining a method in which the number of steps in a circuit design is determined

Atty Docket No. 10K119181
Date Mailed 11/16/01
Attorney

The U.S. Patent & Trademark Office hereby acknowledges receipt of the following:

<input checked="" type="checkbox"/> Application (Utility <input checked="" type="checkbox"/> or Design)	<input checked="" type="checkbox"/> Total Pages <u>44</u>
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/015,209	11/23/2001 11/16/2001	2812	740	NEKU 19.181	14	20	3

CONFIRMATION NO. 5984

026304
ROSENMAN & COLIN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

FILING RECEIPT



OC000000007285532

Date Mailed: 01/10/2002

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Eiki Hashimoto, Kanagawa, JAPAN;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 354306/2000 11/21/2000

If Required, Foreign Filing License Granted 01/09/2002

Projected Publication Date: 05/23/2002

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor circuit designing apparatus and a semiconductor circuit designing method in which the number of steps in a circuit design and a layout design is reduced

Preliminary Class

438

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